GPS RF FRONT END IC WITH PROGRAMMABLE FREQUENCY SYNTHESIZER FOR USE IN WIRELESS PHONES

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims priority under 35 U. S. C. § 119(e) of United States Provisional Patent Application No. 60/229,839, filed August 31, 2000, entitled "GPS RF FRONT END IC WITH PROGRAMMABLE FREQUENCY SYNTHESIZER FOR USE IN WIRELESS PHONES," by Robert Tso et al., which application is incorporated by reference herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention.

The present invention relates in general to Global Positioning System (GPS) receivers, and in particular to a GPS Radio Frequency (RF) front end integrated circuit (IC) with a programmable frequency synthesizer.

2. Description of the Related Art.

U.S. Patent No. 6,041,222, which is herein incorporated by reference, describes a method of using a common reference signal for both GPS and wireless subsystems, but does not present a method which is compatible with the frequency requirements of U.S. Patent No. 5,897,605, which is herein incorporated by reference.

SUMMARY OF THE INVENTION

To minimize the limitations in the prior art, and to minimize other limitations that will become apparent upon reading and understanding the present specification, the present invention discloses a GPS RF Front End IC, containing a Programmable Frequency synthesizer which allows for a relatively fixed internal frequency plan while able to use a number of different reference frequencies provided by the host platform, which can be a wireless telephone device, or other such device, which can provide an accurate reference frequency signal.

An object of the present invention is to provide a GPS RF front end that can accept different reference frequencies allowing a common frequency reference to be used by the GPS receiver and the host device, such as a wireless transceiver.

BRIEF DESCRIPTION OF THE DRAWINGS

Referring now to the drawings in which like reference numbers represent corresponding parts throughout:

FIG. 1 illustrates a wireless mobile terminal wherein a common Reference Frequency Oscillator used to provide a common Reference Frequency Signal to both a GPS Front End Frequency synthesizer, and to a Wireless Transceiver Frequency Synthesizer; and

FIG. 2 illustrates an implementation of the GPS Frequency Synthesizer in accordance with the present invention.

DETAILED DESCRIPTION OF THE INVENTION

In the following description of the preferred embodiment, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration a specific embodiment in which the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present invention.

Overview

This invention when combined with the receiver described in U.S. Patent No. 5,897,605 comprise a GPS Receiver chip set which forms the core of a complete GPS receiver.

The spread spectrum receiver of U.S. Patent No. 5,897,605 processes GPS sampled data at 48fo. The invention described herein provides clocks and sampled data at rates compatible with the requirements of this receiver for a wide variety of commonly used reference frequencies, such as those available in host products like cellular telephones, two way pagers, etc. This is important since it allows the same GPS chip set to be used in a number of different wireless handsets with different standards and reference frequencies without redesigning the frequency inputs to the chipset, as well as eliminating the requirement for multiple crystals within the GPS receiver.

The LO frequency (F_{LO}) is generated by the Programmable Frequency Synthesizer of the present invention, which can be implemented in at least two ways described below: 1) M/N 2) Fractional-N.

Method 1: M/N

Table 1 below provides the values of M and N that will generate an LO which places the IF center at approximately 9 1/3 fo. The Synthesizer uses programmable counters M and N. The frequency plan assumes that LO is approximately F_{LO} = (1540 – 9 1/3)xfo, where fo = 1.023MHz.

Table 1. M/N Frequency Synthesizer design parameters for Commonly used Wireless reference frequencies.

Reference Frequency	M (Feedback divider)	N (Ref divider)
13.0 MHz	4336(=16x271)	36
26 MHz	4336	72
15.36 MHz	3568(=16x223)	35
16.8 MHz	3728(=16x233)	40
19.2 MHz	2528(=16x158)	31
19.68 MHz	2816(=16x179)	36
12.00 MHz	4176 (=16x261)	32

Method 2: Fractional-N

The Fractional-N synthesizer uses a DIV-4 prescaler, with output as the input clock of the M divider. The M divider includes a pulse swallow function, which effectively results in dividing by M+1 in the event that a clock pulse is swallowed. The rate at which M+1 mode is active is controlled by the overflow bit of an 8-bit accumulator, which has a programmable addend. For example, in the case of 13MHz reference, a divide-2 prescaler is used to create a reference at 6.5MHz. This needs to be multiplied up by 60.2258. Since an 8-bit accumulator is used, this is approximated by using an addend of 58, which results in an apparent doppler of 19kHz. It is advantageous in order to simplify GPS software to have a frequency plan where the frequency error or "doppler" is always of one polarity, has limited magnitude (<200kHz) and is not close to zero with some reasonable margin (10kHz). Table 2 provides the Fractional N frequency plan for use with commonly used wireless reference frequencies.

Table 2. Fractional N Frequency Plan for commonly used Wireless reference frequencies.

Ref Freq	Div N	Fref	M(float)	Frac	8-bit add	M-implement	Flo	Fdoppler(kHz)
13	2	6.5	60.2258	0.2258	58	60.2266	1,565.89	19
26	4	6.5	60.2258	0.2258	58	60.2266	1,565.89	19
15.36	3	5.12	76.4586	0.4586	118	76.4609	1,565.92	48
16.8	3	5.6	69.9050	0.9050	232	69.9063	1,565.90	28
19.2	3	6.4	61.1669	0.1669	43	61.1680	1,565.90	28
19.68	3	6.56	59.6750	0.6750	173	59.6758	1,565.89	20

Detailed Description

FIG. 1 illustrates a wireless mobile terminal wherein a common Reference Frequency Oscillator used to provide a common Reference Frequency Signal to both a GPS Front End Frequency synthesizer, and to a Wireless Transceiver Frequency Synthesizer. The Frequency Synthesizer within the GPS Front End generates an LO signal which is used to down convert the GPS bearing signals to a lower frequency IF signal. The GPS Frequency Synthesizer also generates clocking signals ACQCLK and GPSCLK for usage by the digital section of the GPS Receiver.

FIG. 2 illustrates one implementation of the GPS Frequency Synthesizer. A VCO is controlled by a Phase Lock Loop (PLL) to produce and maintain an LO signal with frequency near 1566 MHz. This LO signal is used by the down-converting mixer(s) of the GPS Front End. It is also provided to a DIV-41 counter used to generate the ACQCLK signal, and to a DIV 31-8/9th counter to generate the GPSCLK signal. The DIV 31-8/9th counter also provides a LO/4 output signal which is used by the PLL to phase lock the VCO output signal (LO) to the Reference Frequency Signal (REF).

ACQCLK Synthesis

The DIV-41 counter used to synthesize ACQCLK is a dual-modulus type counter, which is well known to practitioners in the art of electronic Frequency Synthesis. The DIV-41 is comprised of a DIV-3/4 prescaler inputting the LO signal and outputting a reduced frequency signal X1, which is coupled to the input of a DIV-11 counter, which in turn produces the ACQCLK signal at its output. A Select 3-or-4 function controls the state of DIV-3/4 so it divides by 3 or divides by 4 as required to obtain an overall divide ratio of 41. The SEL block is implemented by delay gates and flip-flops for re-timing, which has inputs LO, X1 and X2. The divide factor of 41 is obtained by dividing by 4 for 8 states, followed by dividing by 3 for 3 states of the DIV-11 counter. So, counting LO cycles, we have (4x8) + (3x3) = (32)+(9) = 41 LO cycles before the output of the DIV-11 repeats, which is the desired behavior to obtain the proper divide ratio. Other dual-modulus schemes are possible to implement a DIV-41 function, such as DIV-5/6 driving a DIV8, where divide by 5 is active for 7 states, followed by divide by 6 for the 1 remaining state of DIV8. In this case, we would have (5x7) + (6x1) = (35)+(6) = 41. Another possible implementation uses a DIV4, providing 4 output phases into a 4:1 mux. The mux output drives the input of a DIV-10 counter. A phase select counter retards the phase by 90 degrees, every time the DIV-10 counter completes a cycle, and produces a rising or falling edge. The advantage of this 3rd implementation is that it shares a common DIV-4 element with that used for the GPSCLK Synthesis, which lowers power dissipation and die area.

GPSCLK Synthesis

The GPSCLK is synthesized by using a simple fractional-N method. The effective divide ratio here is a value between 31 and 32. More specifically this invention achieves an effective time

averaged divider ratio of 31 and 8/9ths. The manner by which this is achieved is as follows. The LO signal is first divided down by a DIV-4 prescaler, configured to have 4 outputs, each output having a 90 degree phase relationship with one of the other outputs. One can think of the 4 outputs as having 0, 90, 180, and 270 degrees of phase shift. A 4-to-1 mux is used to periodically *advance* the phase of the input signal to the DIV-8 counter. When it occurs, the phase advancement causes the subsequent DIV-8 counter to advance its state changes by exactly one LO period. The output of the DIV-8 counter drives the input of a DIV-9 counter, which in turn drives a DIV-4 state counter, which in turn is used to produce a mux SEL signal for the 4:1 mux. The operation is as follows: The counter spends most of its time in DIV-32 mode. The mux SEL signal is constant for 8 of the 9 phase states of the DIV-9 counter. When the DIV-9 counter outputs a rising edge, a DIV-4 state counter is toggled, which causes the 4:1 mux to advance the phase of the 4:1 mux output, which is coupled to the DIV-8 input. Since this causes the DIV-8 output to toggle one LO period sooner, effectively the divide value becomes 31 instead of 32. Thus, we have a divider pattern of divide by 32, 8 times, followed by divide by 31 once, and then repeating. The time averaged divide ratio would thus be calculated as: [(32x8) + (31x1)] / 9 = [256 + 31] /9 = 287/9 = 31 8/9ths. In other words, the GPSCLK output signal waveform would contain 8 cycles that are slightly "too long" (generated by divide by 32) followed by a cycle that is "too short" (generated by divide by 31) so that over the average of 9 cycles, the frequency of GPSCLK is exactly as required. For the GPS frequency plan where the frequency of GPSCLK is about 49.107 MHz, the time domain"error" in the long and short cycles is about 71 psec and –568 psec respectively.

Programmability to Accept Various Reference Frequency Signals:

The remaining portion of the Frequency Synthesizer not discussed above serves to allow the VCO to be phase locked to a number of Reference Frequency (REF) signals having different frequencies. This is achieved by using a technique well known to practitioners in the art of electronic frequency synthesis as "M-over-N" synthesis. The REF signal is inputted to a programmable modulus divider DIV-N which provides the "R" input of the Phase Frequency Detector (PFD). The LO/4 signal is inputted to a DIV-4 counter, the output of which is the input of a programmable modulus DIV-M counter. The output of the DIV-M counter is the "V" input of the PFD. The outputs of the PFD are coupled to the inputs of a Charge Pump (CP) circuit. The output of the CP circuit is coupled to a Loop Filter, which is also coupled to the control input of the VCO, thus providing the feedback signal needed to"close the loop" of the PLL.

The DIV-N counter is implemented as a 7-bit count-down counter, so that divide ratios from 128 to 2 can be programmed for DIV-N. The DIV-M counter is implemented as a 9-bit count-down counter, so that divide ratios from 512 to 2 can be programmed for DIV-M. Other implementations are possible by simply extending the size of the counters, however the implementation disclosed is adequate for the range of REF frequencies in Table 1, given the frequency offset constraints of the GPS receiver disclosed in US # 5,897,605.

GPS receivers are typically limited to operate using a fixed frequency plan. The selection of "N" and "M" divide values is done with the criteria of choosing the lowest values of "N" and "M" that produces an LO frequency that results in a substantially small frequency offset which can be accommodated by the GPS receiver. Small values of "N" and "M" are desired to maximize the PLL reference frequency and to maximize the available loop gain of the PLL

Conclusion

In summary, a GPS RF front end with programmable synthesizer is disclosed. A GPS RF Front End in accordance with the present invention comprises a Voltage Controlled Oscillator (VCO) for producing a Local Oscillator (LO) signal, wherein the LO signal has a frequency at approximately 1566 MHz, a first fixed counter means, coupled to the VCO, for dividing the LO signal frequency by 41, to obtain a second signal with frequency of LO/41, wherein the second signal is an ACQCLK signal, a second fixed counter means, coupled to the VCO, for dividing the LO signal by 31-and-8/9ths, to obtain a third signal with frequency of 9/7 times the frequency of the second signal, wherein the second signal is a GPSCLK signal, the second fixed counter means further comprising a first divide-by-4 counter, the first divide-by-4 counter having five outputs, each output having a frequency of LO/4, a second divide-by-4 counter, coupled to one of the five outputs of the first divide-by-4 counter, a first programmable count-down counter, coupled to the output of the second divide-by-4 counter, a second programmable count-down counter, coupled to a Reference Frequency Signal, the Reference Frequency Signal being used by the wireless mobile terminal, and a Phase Frequency Detector, coupled to the outputs of the first and second programmable count-down counters, for comparing the phase and frequency of the outputs of the first and second programmable count-down counters.

The foregoing description of the preferred embodiment of the invention has been presented for the purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed. Many modifications and variations are possible in light of the above teaching. It is intended that the scope of the invention not be limited by this detailed description, but by the claims appended hereto.